The patent applicants would first like to explain to the patent examiner, how LLS (Localized Light Scattering) defects are defined in the context of their patent application.

LLS defects are defined as light scattering defects, as measured with light scattering tools like Tencor SP1 or similar tools. These tools measure the scattered light due to defects on top of the wafer surface, which may be either pits or particles. The patent application therefore relates to these defects on the top surface of the epitaxial layer and not to the bottom surface, which is the interface between epitaxial layer and wafer substrate.

In the following, the patent applicants would like to explain in more detail where the difficulties lie in reducing the number of LLS and why it is not expected or obvious to reach low LLS in combination with thin epitaxial layers.

The patent applicants will show, that achieving low LLS numbers when using Epi thicknesses thicker than stated in their patent, does not require special know-how and is state-of-the art for silicon epitaxial layer deposition on silicon substrate wafers.

The main challenge for achieving low LLS at thin epitaxial layers at or below one micron is to avoid that the underlying COP (Crystal Originated Particle) defects in the substrate wafer get imprinted through the epitaxial layer and become visible at the top surface. The COP defects originate from crystal pulling, and are especially abundant for fast pulled / fast cooled substrates, as they are described by the patent applicants. Fast pulled ingots allow to reduce production costs significantly compared to standard or slow pulled material and are therefore the preferred material for the production of silicon wafer substrates.

Figure 1 shows a typical COP defect (largely magnified, see the scale) in a silicon substrate wafer. The COP is a small void in the silicon substrate and has an octahedral shape. The COP shown is at the wafer surface and can be detected after delineation during wafer polishing. The patent examiner should note, that there are also COPs below the wafer surface, which however, for the current invention, are of no relevance.

For their invention, the patent applicants were using specifically fast pulled / cooled and nitrogen co-doped ingot material. Nitrogen co-doping has the advantage, that the COPs become smaller than in material which is not Nitrogen co-doped.

Figure 2 shows the positive shrinking effect on the COP size when using nitrogen co-doping.

Depositing an epitaxial layer on a silicon substrate wafer, as shown in Figure 2, normally leads to high LLS counts, especially for thin epi layers and small LLS. This is because, after epitaxial deposition, the COPs leave their fingerprints on top of the surface layer in the form of more or less shallow defects on the surface. The effect gets more and more pronounced, the thinner the epitaxial layer.

Figure 3 shows how the LLS density for LLS >0.085um size increase by several orders of magnitude, when going to epi thicknessess smaller than 1um. The data are

from the patent applicants, but could also be taken from any other suitable sources to be found in the literature, as they just describe the behaviour of standard silicon substrates, on which standard silicon epitaxy is performed.

It is obvious from the numbers in Figure 3, that typical LLS numbers >0.085um for epitaxial layer thicknesses in the range of 0.2 – 1.0um, which are the subject of the current patent application, are of the order 100 – 1000, which is much higher than the claimed 30 LLS.

In order to achieve such low LLS numbers for thin epitaxial layers, the patent applicants had to invent a new combination of ingot pulling process (in order to have sufficient small COPs in the substrate) and epitaxial layer deposition.

Figure 4 shows the extremely shallow defects remaining on the wafer surface when using the patents applicants process, which lead to the very low LLS numbers which could be achieved with this new product.

Regarding the patent as issued by Wijaranakula et al., the patent applicants would like to point out, that this invention does not relate to the current patent application.

First, this is because Wijaranakula et al. have invented a method to produce silicon wafers, which uses ion implantation. Ion implantation however is not able to reduce the size of the COPs in the underlying substrate nor to make them vanish. This is because implantation is not able to fill the voids with oxygen or nitrogen (which would be the only way one could think of, the COPs could vanish by implantation).

Secondly, all examples of Wijaranakula et al. relate to 1.6um epitaxial layer thickness. As the patent applicants have shown above (see Figure 3), producing an epitaxial wafer with this epi thickness and low LLS, is not surprising and simply state-of-the art. Wijaranakula et al. therefore describe another product as the current invention, which is for thin epitaxial layers.

Regarding the patent of Graef et al., the patent applicants would like to state, that the temperature ranges described therein (above 1000°C) are completely different than the temperature ranges described by Wijaranakula et al. Wijaranakula et al. use an annealing step in order to enhance the growth of precipitates and therefore the gettering in the substrate, which however can only be achieved at temperatures significantly lower (about 700-800°C). It is therefore not possible to combine both the Graef et al. and Wijaranakula et al. patents.

The patent applicants hope to have clarified all open questions, the patent examiner had. The above explanations should be sufficient to proove, that the invention was not obvious and could not be made by simply combining the cited patents. The patent applicants therefore also do not think, that a test program, as proposed, would supply additional evidence. In case there still should be additional questions, the patent applicants are of course to the full disposal of the patent examiner.

Figure 1: Typical COP, leading to LLS defects on the wafer surface

Polishing: mechanism of void delineation

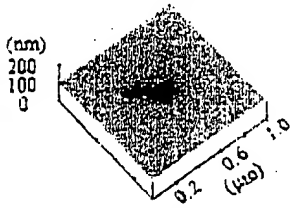
TEM image of octahedral void

Delineation of void

M. Isaka, H. Akiyo, T. Ueki, M. Tomita, M. Yamaguchi, Jpn. J. Appl. Phys. 35 (1996) 812.

H. Zenger, J. Vanhellemont, P. Schmuck, Jpn. J. Appl. Phys. 36 (1997) 217.

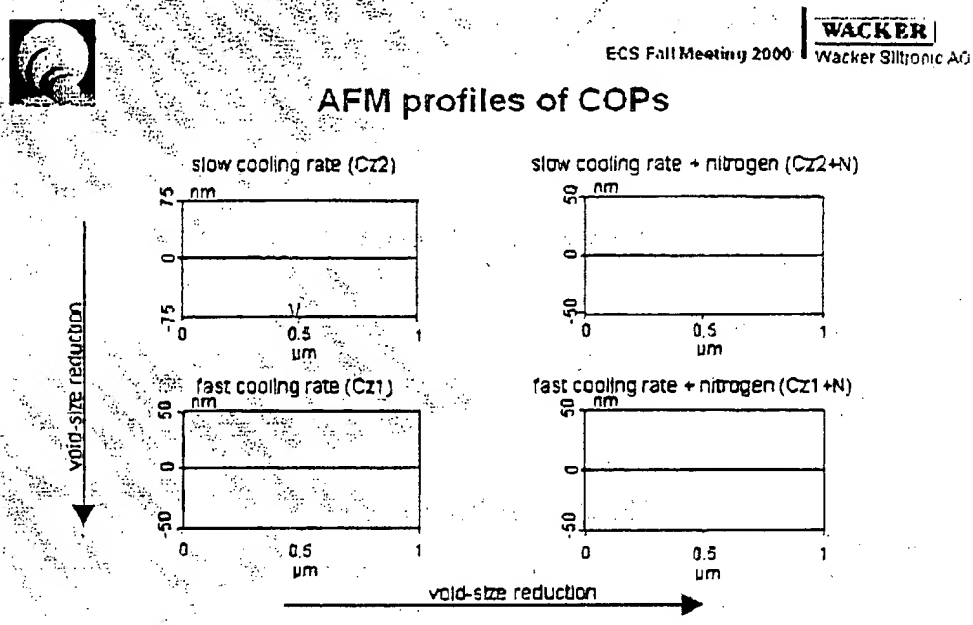
AFM image of LLS delineated by polishing: COP



P. Schmuki, D. Gräf, The Electrochem. Soc. PV98-1 (1998) 276

- voids delineated by polishing: COPs, J. Ryuta, E. Morita, T. Tanaka, Y. Shimanuki, Jpn. J. Appl. Phys. 29 (1990) L1947.)
- LLSs on polished wafers comprise COPs
- number of COPs/LLSs observed after polishing for a specific wafer is independent of stock removal (polishing "does not integrate")

Figure 2: Shrinking of COP sizes (and simultaneous COP density increase) with increasing nitrogen co-doping concentration and/or increasing cooling rate



200 mm Cz p⁻ material
in case of nitrogen doping: [N] ~ $3 \cdot 10^{14}$/cm^3

Figure 3: Strong increase of LLS defects > 0.085um for Epi thicknesses smaller than 1um and standard Epi wafers

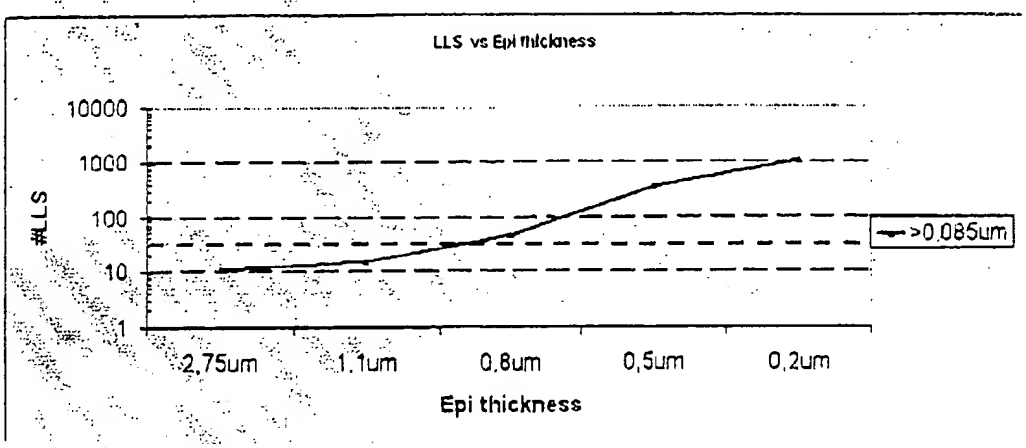


Figure 4: Remaining, extremely shallow defects on the epitaxial wafer surface for the new wafers claimed by the patent applicants; these extremely shallow defects lead to very low LLS numbers